HERMETIC PACKAGES AND FEEDTHROUGHS FOR NEURAL PROSTHESES

Quarterly Progress Report # 9

(Contract NIH-NINDS-N01-NS-4-2319)

(Contractor: The Regents of the University of Michigan)

For the Period:

October-December 1996

Submitted to the

Neural Prosthesis Program
National Institute of Neurological Disorders and Stroke
National Institutes of Health

By the

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December 1996

SUMMARY

During the past quarter we continued testing of glass packages under accelerated conditions, started the testing and characterization of the receiver circuitry for the single-channel microstimulator as well as the new fully-integrated microstimulator that has no hybrid components and requires a small package for peripheral nerve stimulation, and characterized the performance of on-chip coils for power and data transfer in integrated systems.

Our most significant package testing results to date are those obtained from a series of silicon-glass packages that have been soaking in DI water at 85°C and 95°C for more than a year. We reported in the last progress reports that all packages soaking at 95°C had failed. There were also 4 packages that were soaking at 85°C. All these four packages are still dry and under test. Of the original 10 packages, the longest going sample has reached a maximum of 869 days at 85°C and 484 days at 95°C. If we assume that all of the packages at 85°C failed the same time that the 95°C packages failed (obviously this is not the case, but for purposes of obtaining a more realistic mean time to failure for these packages we make this assumption), we can calculate a worst case mean time to failure of 258 days for the samples at 85°C, and of 119 days for the samples soaking at 95°C. The worst case MTTF at body temperature based on these tests is then calculated to be 59 years. These tests have been very encouraging and clearly indicate the packages can last for many years in water. In addition to these tests in DI water, we had also soaked several packages in ***saline*** at the above two temperatures. The results obtained from these tests were reported in the last progress report. We will continue to perform high-temperature tests in saline in the coming quarter once we have determined an effective way of preventing silicon dissolution at these higher temperatures. We also have had 4 packages soaking at room temperature in saline. The longest lasting package has been soaking for 770 days, and an average soak period of 641 days at room temperature. We will continue to observe these packages for any sign of leakage.

We have also fabricated a low-profile glass package (with a total thickness of less than 1mm) for use in fully integrated microstimulator systems. Four sample silicon-glass packages were fabricated and sent to Johns Hopkins University for testing and evaluation.

During the past quarter we completed the fabrication of the receiver circuitry for the microstimulator. This circuitry underwent substantial testing and characterization during this past quarter. The results of this testing have been rather disappointing because we have been observing a consistently large leakage current in the microstimulator circuitry. A large number of tests have been performed on this circuitry to locate the source of this leakage, including full characterization of device characteristics, monitoring surface and junction leakage, verifying circuit layout and checking design rules, and measuring doping profile and concentration in the silicon substrates. None of these seem to indicate any cause for a large leakage current. Therefore, at this point we still cannot say why the circuits show such a large leakage. We will continue our tests full force in the coming quarter and will determine the cause of leakage, and will fix this problem in the coming quarter.

Finally, during the past quarter we also tested the circuitry for a fully integrated mini-microstimulator that can operate using on-chip coils. This circuitry was shown to be fully functional in the last progress report, although it consumed too much current. The source of this high current consumption was determined to be a layout error that can be easily fixed. In addition, we fabricated a large number of on-chip copper coils and have shown that on-chip inductances of several micro Henry can be easily obtained. This allows the on-chip coils to be tuned using on-chip capacitors. In addition, these coils can receive several tens of milliwatts of power from an external coil located several centimeters from the receiver coil. This demonstrates that it is possible to eliminate the hybrid coil and capacitor in the microstimulator, thus significantly reducing the overall dimensions of the device, which is desirable for applications involving peripheral nerve stimulation.

1. INTRODUCTION

This project deals with the development of hermetic, biocompatible micropackages and feedthroughs for use in a variety of implantable neural prostheses for sensory and motor handicapped individuals. The project also aims at continuing work on the development of a telemetrically powered and controlled neuromuscular microstimulator for functional electrical stimulation. The primary objectives of the project are: 1) the development and characterization of hermetic packages for miniature, silicon-based, implantable three-dimensional structures designed to interface with the nervous system for periods of up to 40 years; 2) the development of techniques for providing multiple sealed feedthroughs for the hermetic package; 3) the development of custom-designed packages and systems used in chronic stimulation or recording in the central or peripheral nervous systems in collaboration and cooperation with groups actively involved in developing such systems; and 4) establishing the functionality and biocompatibility of these custom-designed packages in *in-vivo* applications. Although the project is focused on the development of the packages and feedthroughs, it also aims at the development of inductively powered systems that can be used in many implantable recording/stimulation devices in general, and of multichannel microstimulators for functional neuromuscular stimulation in particular.

Our group here at the Center for Integrated Sensors and Circuits at the University of Michigan has been involved in the development of silicon-based multichannel recording and stimulating microprobes for use in the central and peripheral nervous systems. More specifically, during the past two contract periods dealing with the development of a single-channel inductively powered microstimulator, our research and development program has made considerable progress in a number of areas related to the above goals. A hermetic packaging technique based on electrostatic bonding of a custom-made glass capsule and a supporting silicon substrate has been developed and has been shown to be hermetic for a period of at least a few years in salt water environments. This technique allows the transfer of multiple interconnect leads between electronic circuitry and hybrid components located in the sealed interior of the capsule and electrodes located outside of the capsule. The glass capsule can be fabricated using a variety of materials and can be made to have arbitrary dimensions as small as 1.8mm in diameter. A multiple sealed feedthrough technology has been developed that allows the transfer of electrical signals through polysilicon conductor lines located on a silicon support substrate. Many feedthroughs can be fabricated in a small area. The packaging and feedthrough techniques utilize biocompatible materials and can be integrated with a variety of micromachined silicon structures.

The general requirements of the hermetic packages and feedthroughs to be developed under this project are summarized in Table 1. Under this project we will concentrate our efforts to satisfy these requirements and to achieve the goals outlined above. There are a variety of neural prostheses used in different applications, each having different requirements for the package, the feedthroughs, and the particular system application. The overall goal of the program is to develop a miniature hermetic package that can seal a variety of electronic components such as capacitors and coils, and integrated circuits and sensors (in particular electrodes) used in neural prostheses. Although the applications are different, it is possible to identify a number of common requirements in all of these applications in addition to those requirements listed in Table 1. The packaging and feedthrough technology should be capable of:

1- protecting non-planar electronic components such as capacitors and coils, which typically have large dimensions of about a few millimeters, without damaging them;
2- protecting circuit chips that are either integrated monolithically or attached in a hybrid fashion with the substrate that supports the sensors used in the implant;
3- interfacing with structures that contain either thin-film silicon microelectrodes or conventional microelectrodes that are attached to the structure;

Table 1: General Requirements for Miniature Hermetic Packages and Feedthroughs for Neural Prostheses Applications

Package Lifetime:

≥ 40 Years in Biological Environments @ 37°C

Packaging Temperature:

≤360°C

Package Volume:

10-100 cubic millimeters

Package Material:

Biocompatible
Transparent to Light
Transparent to RF Signals

Package Technology:

Batch Manufactureable

Package Testability:

Capable of Remote Monitoring
In-Situ Sensors (Humidity & Others)

Feedthroughs:

At Least 12 with ≤125μm Pitch
Compatible with Integrated or Hybrid Microelectrodes
Sealed Against Leakage

Testing Protocols:

In-Vitro Under Accelerated Conditions
In-Vivo in Chronic Recording/Stimulation Applications

We have identified two general categories of packages that need to be developed for implantable neural prostheses. The first deals with those systems that contain large components like capacitors, coils, and perhaps hybrid integrated circuit chips. The second deals with those systems that contain only integrated circuit chips that are either integrated in the substrate or are attached in a hybrid fashion to the system.

Figure 1 shows our general proposed approach for the package required in the first category. This figure shows top and cross-sectional views of our proposed approach here. The package is a glass capsule that is electrostatically sealed to a support silicon substrate. Inside the glass capsule are housed all of the necessary components for the system. The electronic circuitry needed for any analog or digital circuit functions is either fabricated on a separate circuit chip that is hybrid mounted on the silicon substrate and electrically connected to the silicon substrate, or integrated monolithically in the support silicon substrate itself. The attachment of the hybrid IC chip to the silicon substrate can be performed using a number of different technologies such as simple wire bonding between pads located on each substrate, or using more sophisticated techniques such as flip-chip solder reflow or tab bonding. The larger capacitor or microcoil components are mounted on either the substrate or the IC chip using appropriate epoxies or solders. This completes the assembly of the electronic components of the system and it should be possible to test the system electronically at this point before the package is completed. After testing, the system is packaged by placing the glass capsule over the entire system and bonding it to the silicon substrate using an electrostatic sealing process. The cavity inside the glass package is now hermetically sealed against the outside environment. Feedthroughs to the outside world are provided using the grid-feedthrough technique discussed in previous reports. These feedthroughs transfer the electrical signals between the electronics inside the package and various elements outside of the package. If the package has to interface with conventional microelectrodes, these microelectrodes can be attached to bonding pads located outside of the package; the bond junctions will have to be protected from the external environment using various polymeric encapsulants. If the package has to interface with on-chip electrodes, it can do so by integrating the electrode on the silicon support substrate. Interconnection is simply achieved using on-chip polysilicon conductors that make the feedthroughs themselves. If the package has to interface with remotely located recording or stimulating electrodes that are attached to the package using a silicon ribbon cable, it can do so by integrating the cable and the electrodes again with the silicon support substrate that houses the package and the electronic components within it.

Figure 2 shows our proposed approach to package development for the second category of applications. In these applications, there are no large components such as capacitors and coils. The only component that needs to be hermetically protected is the electronic circuitry. This circuitry is either monolithically fabricated in the silicon substrate that supports the electrodes (similar to the active multichannel probes being developed by the Michigan group), or is hybrid attached to the silicon substrate that supports the electrodes (like the passive probes being developed by the Michigan group). In both of these cases the package is again another glass capsule that is electrostatically sealed to the silicon substrate. Notice that in this case, the glass package need not be a high profile capsule, but rather it need only have a cavity that is deep enough to allow for the silicon chip to reside within it. Note that although the silicon IC chip is originally 500μm thick, it can be thinned down to about 100μm, or can be recessed in a cavity created in the silicon substrate itself. In either case, the recess in the glass is less than 100μm deep (as opposed to several millimeters for the glass capsule). Such a glass package can be easily fabricated in a batch process from a larger glass wafer.

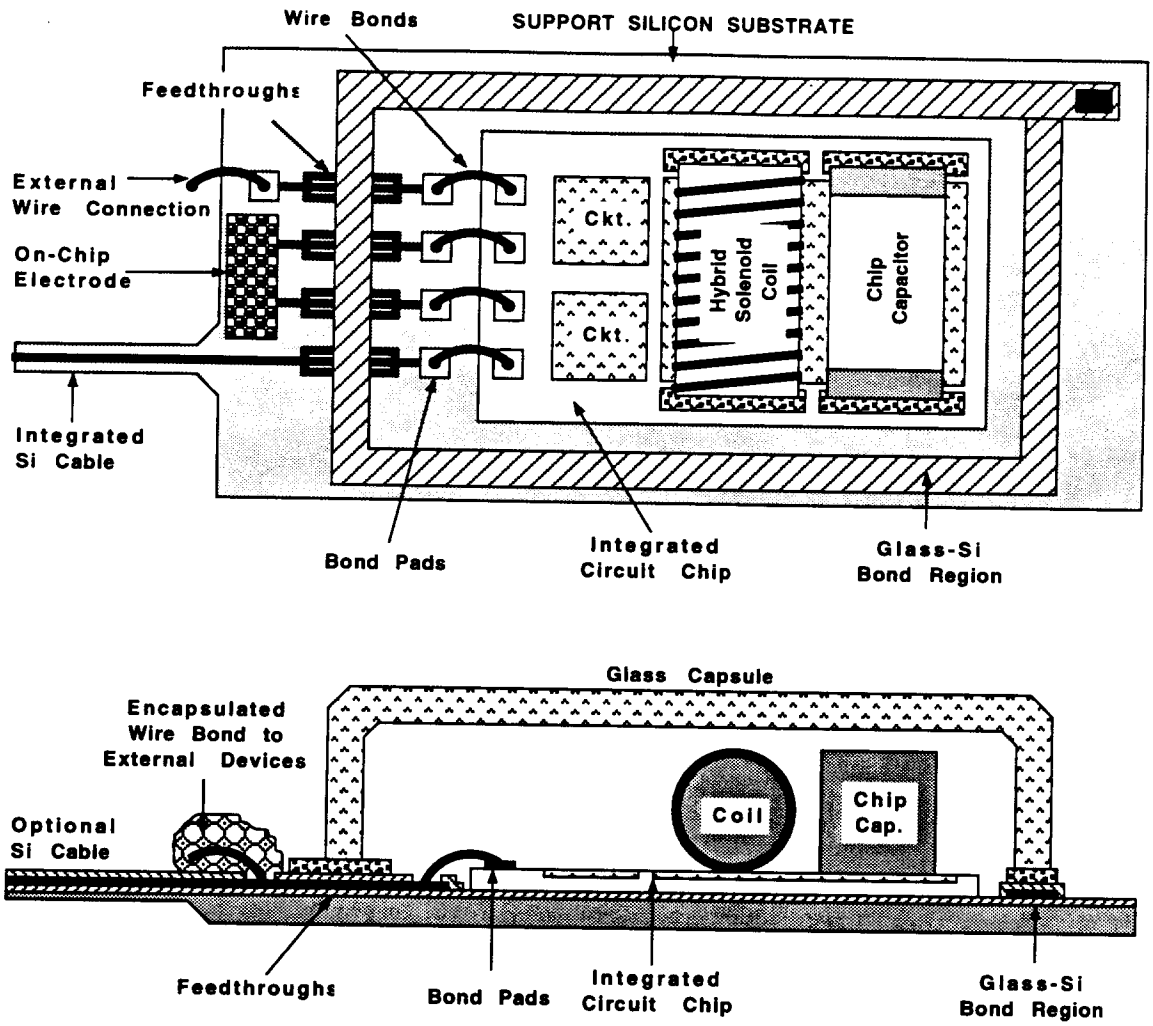

Figure 1: A generic approach for packaging implantable neural prostheses that contain a variety of components such as chip capacitors, microcoils, and integrated circuit chips. This packaging approach allows for connecting to a variety of electrodes.

We believe the above two approaches address the needs for most implantable neural prostheses. Note that both of these techniques utilize a silicon substrate as the supporting base, and are not directly applicable to structures that use other materials such as ceramics or metals. Although this may seem a limitation at first, we believe that the use of silicon is, in fact, an advantage because it provides several benefits. First, it is biocompatible and has been used extensively in biological applications. Second, there is a great deal of effort in the IC industry in the development of multi-chip modules (MCMs), and many of these efforts use silicon supports because of the ability to form high density interconnections on silicon using standard IC fabrication techniques. Third, many present and future implantable probes are based on silicon micromachining technology; the use of our proposed packaging technology is inherently compatible with most of these probes, which simplifies the overall structure and reduces its size.

Once the above packages are developed, we will test them in biological environments by designing packages for specific applications. One of these applications is in recording neural activity from cortex using silicon microprobes developed by the Michigan group under separate contracts. The other involves the chronic stimulation of muscular tissue using a multichannel microstimulator for the stimulation of the paralyzed larynx. This application has been developed at Vanderbilt University. Once the device is built, it will be used by our colleagues at Vanderbilt to perform both biocompatibility tests and functional tests to determine package integrity and suitability and device functionality for the reanimation of the paralyzed larynx. The details of this application will be discussed in future progress reports.

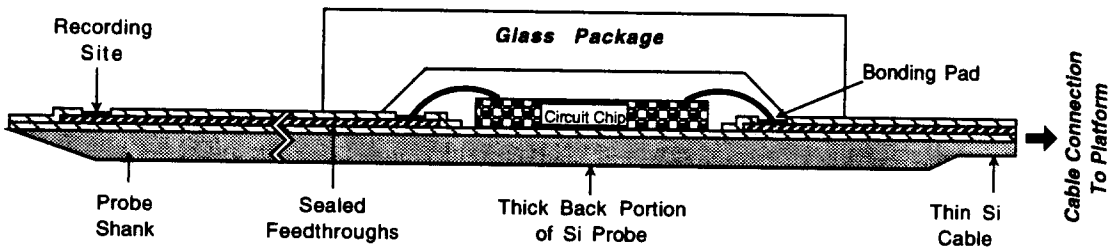

Figure 2: Proposed packaging approach for implantable neural prostheses that contain electronic circuitry, either monolithically fabricated in the probe substrate or hybrid attached to the silicon substrate containing microelectrodes.

2. ACTIVITIES DURING PAST QUARTER

2.1 Hermetic Packaging

Over the past few years we have developed a bio-compatible hermetic package with high density, multiple feedthroughs. This technology utilizes electrostatic bonding of a custom-made glass capsule to a silicon substrate to form a hermetically sealed cavity, as shown in Figure 3. Feedthroughs are obtained by forming closely spaced polysilicon lines and planarizing them with LTO and PSG. The PSG is reflowed at 1100° C for 2 hours to form a planarized surface. A passivation layer of oxide/nitride/oxide is then deposited on top to prevent direct exposure of PSG to moisture. A layer of fine-grain polysilicon (surface roughness 50Å rms) is deposited and doped to act as the bonding surface. Finally, a glass capsule is bonded to this top polysilicon layer by applying a voltage of 2000V between the two for 10 minutes at 320 to 340° C, a temperature compatible with most hybrid components. The glass capsule can be either custom molded from Corning code #7740 glass, or can be batch fabricated using ultrasonic micromachining of #7740 glass wafers.

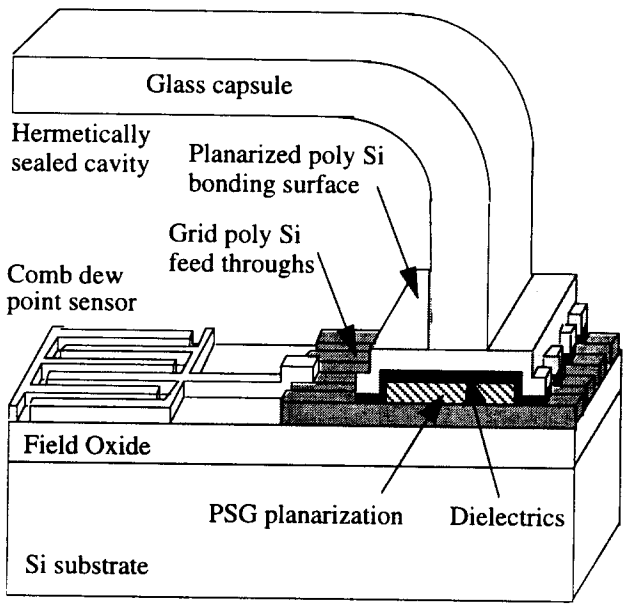

Figure 3: The structure of the hermetic package with grid feedthroughs.

During the past years we have electrostatically bonded and soak tested over one hundred and sixty of these packages. The packages successfully prevent leakage in soak tests at 95° C for over 4 months on average and at 85° C for almost 15 months in deionized water. The bonding yield has varied between 85% to 72% (yield is defined as the percentage of packages which last more than 24 hours soaking in DI water), and in-vivo tests performed so far indicate that the package is bio-compatible and rugged. We also would like to mention that the earlier tests that have been going for more than a year (room temperature soak tests in saline and the 85° C and the 95° C tests in deionized water) have been made with silicon substrates that are thinned (~150μm) and bonded to the custom made glass capsules. The relatively recent tests (85° C and 95° C tests in saline) are performed with the silicon substrates having full thickness (~500μm) and bonded to the ultrasonically machined glass capsules with a flat top surface. During this quarter, we have also made a low profile package that could be used to seal integrated components.

2.1.1 Ongoing Accelerated Soak Tests in Deionized Water

We continued accelerated soak tests during this past quarter. Currently, out of 20 packages that were subjected to soak tests, we have 4 packages that have lasted for more than 2 years with no sign of moisture penetration into them. In these tests temperature is chosen as the accelerating factor since it is easy to control and also diffusion of moisture is a strong(exponential) function of temperature. We had started with 10 samples each soaking at 85° C and 95° C. Tables 2 and 3 list some pertinent data for these soak tests. Figure 4 summarizes the final results from the 95° C soak tests and Figure 5 summarizes the results so far from the 85° C tests. These figures also list the causes of failure for individual packages when it is known, and they show a curve fit to our lifetime data to illustrate the general trend. The curve fit, however, only approximates the actual package lifetimes since some of our packages failed due to breaking during testing rather than due to leakage.

At the beginning of this quarter, we had 4 packages soaking at 85°C. These packages are still dry and being tested. The failure for these packages is defined as room temperature condensation. The testing protocol for these packages consist of cooling the sample to room temperature and then measuring the impedance of the dew point sensors and also inspecting the sample carefully under the microscope. The observation of visible condensation inside the package and the changes in impedance (about 2 orders of magnitude) would both be classified as the failure of the package under test. Of the original 10 samples in the 95°C tests, the longest lasting package survived for a total of 484 days. The calculated mean time to failure of the packages is 135.7 days excluding the handling errors. Of the original 10 packages in the 85° C soak tests there are still 4 with no sign of room temperature condensation with the longest one lasting for more than 869 days. The worst case mean time to failure for these tests has been calculated as 684 days excluding the handling errors. These packages are still under test. We have not yet started testing another set of packages.

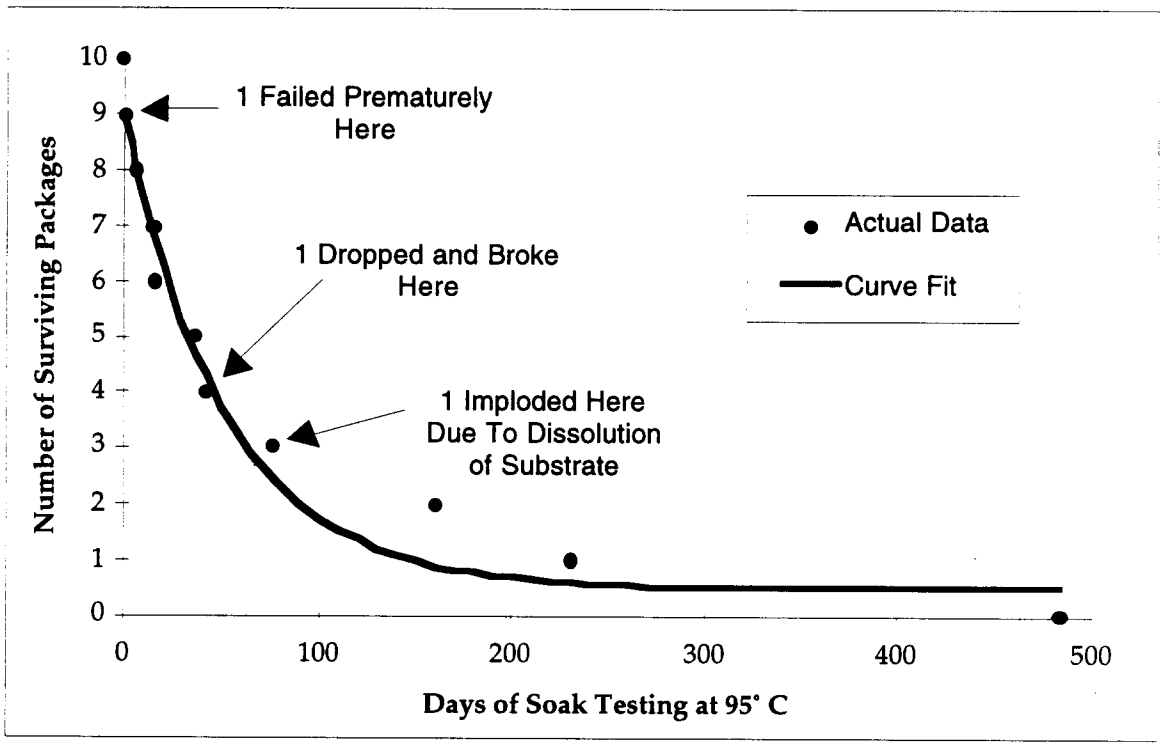

Figure 4: Summary of the lifetimes of the 10 packages which have been soak tested at 95° C in DI water.

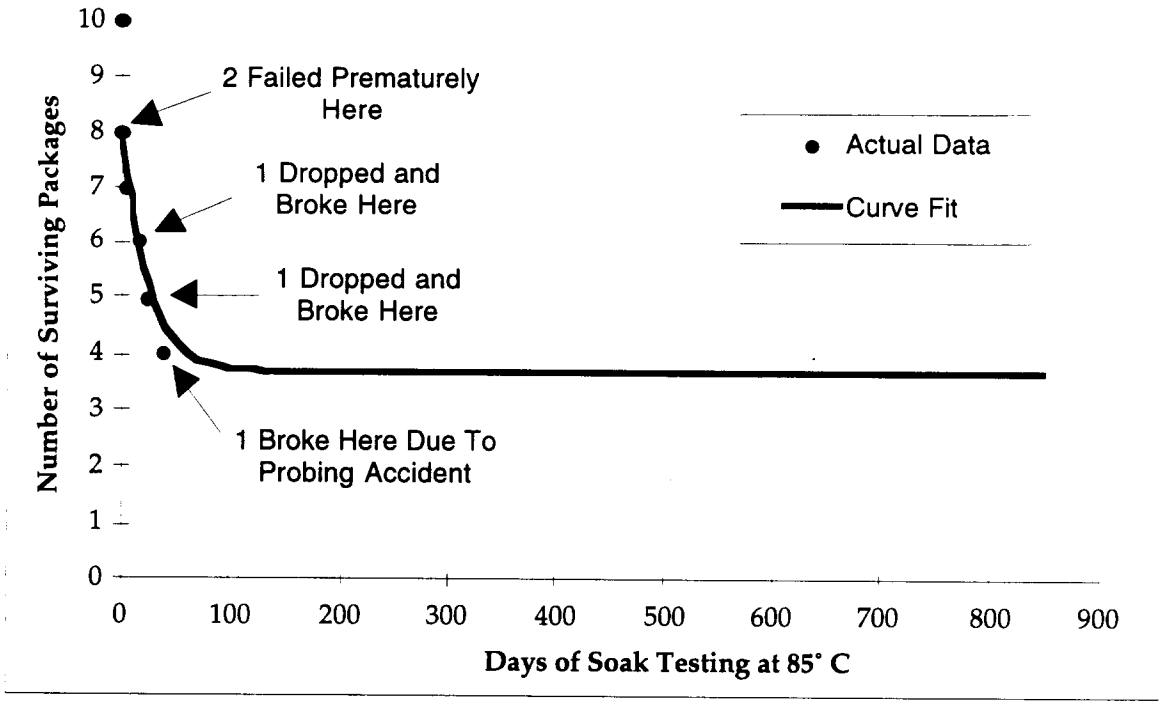

Figure 5: Summary of the lifetimes of the 10 packages which have been soak tested at 85° C in DI water.

Table 2: Key data for 95°C soak tests in DI water.

Number of packages in this study	10
Soaking solution	DI water
Failed within 24 hours (not included in MTTF)	1
Packages lost due to mishandling	2
Longest lasting packages in this study	484 days
Packages still under tests with no measurable room temperature condensation inside	0
Average lifetime to date (MTTF) including losses attributed to mishandling	*118.7 days*
Average lifetime to date (MTTF) not including losses attributed to mishandling	*135.7 days*

Table 3: Key data for 85°C soak tests in DI water.

Number of packages in this study	10
Soaking solution	DI water
Failed within 24 hours (not included in MTTF)	2
Packages lost due to mishandling	3
Longest lasting packages so far in this study	869 days
Packages still under tests with no measurable room temperature condensation inside	4
Average lifetime to date (MTTF) including losses attributed to mishandling	*438.9 days*
Average lifetime to date (MTTF) not including losses attributed to mishandling	*686.4 days*

2.1.2 Interpretation of the Long Term Soak Testing Results in DI Water

We are modeling the mean time to failure (MTTF) as an Arrhenius processes. The generalized equation used is given below where MTTF is the mean time to failure, A is a constant, ξ is the stress factor other than temperature, (such as pressure or relative humidity), n is the stress dependence, Q is the activation energy, K_B is Boltzman's constant, and T is the temperature in Kelvin.

$$MTTF = A \cdot \xi^{-n} \cdot e^{\left(\frac{Q}{K_B T}\right)}$$

For the accelerated soak tests that we have performed on the packages, there was no stressing factor other than temperature, so the ξ term drops out of the above equation. The resulting equation can be rewritten as a ratio of MTTFs as shown below.

$$AF = \frac{MTTF_{Normal}}{MTTF_{Accelerated}} = e^{\frac{Q}{K_B}\left(\frac{1}{T_{Normal}} - \frac{1}{T_{Accelerated}}\right)}$$

By using the current MTTFs at 85°C and 95°C, we can easily calculate the activation energy (Q) and from this activation energy we can proceed to obtain an acceleration factor (AF) for these tests, and then calculate the MTTF at body temperature. Moreover, after analyzing our failed samples we have determined that some of the samples in the 95°C tests have failed prematurely due to increased dissolution of silicon at this temperature. Since dissolution reaction is an exponential function of temperature, the samples at the 85° C tests have been effected less that the ones at 95° C. The model we use only accounts for acceleration of moisture diffusion, but not dissolution. We will still keep and update the data from the samples in the 85° C tests. Since there are no samples soaking at 95°C, and in order to obtain a more realistic MTTF for the packages soaking in

DI water, we assume that all the samples in the 85° C tests have also failed the same time as the longest going sample in the 95° C tests. This assumption will produce the following values:

$$MTTF|_{85°C} = 257.6 Days \quad MTTF|_{95°C} = 118.7 Days$$

Q=0.88 eV, AF(95°C)=179.5, AF(85°C)=82.7

$$MTTF|_{37°C} = 58.4 Years$$

2.1.3 Ongoing Room Temperature Soak Tests

We have been soaking a group of packages in phosphate buffered saline at room temperature for the past 2 years. Table 4 below lists some of the pertinent data from these soak tests. These room temperature soak tests were initiated for two reasons. First, we wanted to have some soak tests in saline and since at higher temperatures we were getting dissolution of silicon in saline, at this temperature we hoped to obtain data without any significant dissolution. Second, we wanted to have some soak data independent of the acceleration technique used. To obtain meaningful data from these tests may take a long time, however the samples in these tests would act as a control group for our accelerated tests.

We started with 6 packages in saline at room temperature. One of these packages failed within one day, most likely due to surface defects or poor bonding due to misalignment. Another one failed after 160 days of soaking. The remaining 4 samples are dry and still under test. These samples, similar to our other samples, are tested visually with the aid of a microscope and electrically with the help of dew point sensors integrated into the package substrate. The longest lasting sample in these tests has reached a total of 770 days and is still being tested. We have calculated a worst case mean time to failure of 641 days.

Table 4: Data for room temperature soak tests in saline.

Number of packages in this study	6
Soaking solution	Saline
Failed within 24 hours (not included in MTTF)	1
Packages lost due to mishandling	1
Longest lasting packages in this study	770 days
Packages still under tests with no measurable room temperature condensation inside	4
Average lifetime to date (MTTF)	*641.2 days*

2.1.4 Fabrication of a Low Profile Package:

In our past progress report we mentioned the possibility of making a package with smaller dimensions for neural stimulation and for use in the next generation microstimulators. This past quarter using our current mask set we fabricated a prototype low profile package. The fabrication sequence is shown in Figure 6. The original thickness of the glass wafers is about 750μm. First, we deposit and pattern Cr/Au layers to act as a mask against the etchant. Next the glass is recessed for a depth of about 40μm in a HF/HNO_3 acid solution. Later, we thin the wafers from the other side to a final thickness of approximately 300μm. The final steps of this process include dicing the glass wafer into small glass capsules and then bonding to our silicon substrate. Figure 7 shows a SEM micrograph of the finished package. For comparison, Figure 8 shows a microstimulator with the standard glass package currently used for encapsulation. For this prototype low profile device, we have used an original microstimulator substrate and have achieved a fairly good seal. These packages were soaked for a duration of several days at 95° C and remained hermetic during that period. We should also add that it is possible to further reduce the thickness of this device by thinning the silicon substrate. Moreover, with the use of a new mask set we can also scale this device in the other dimensions.

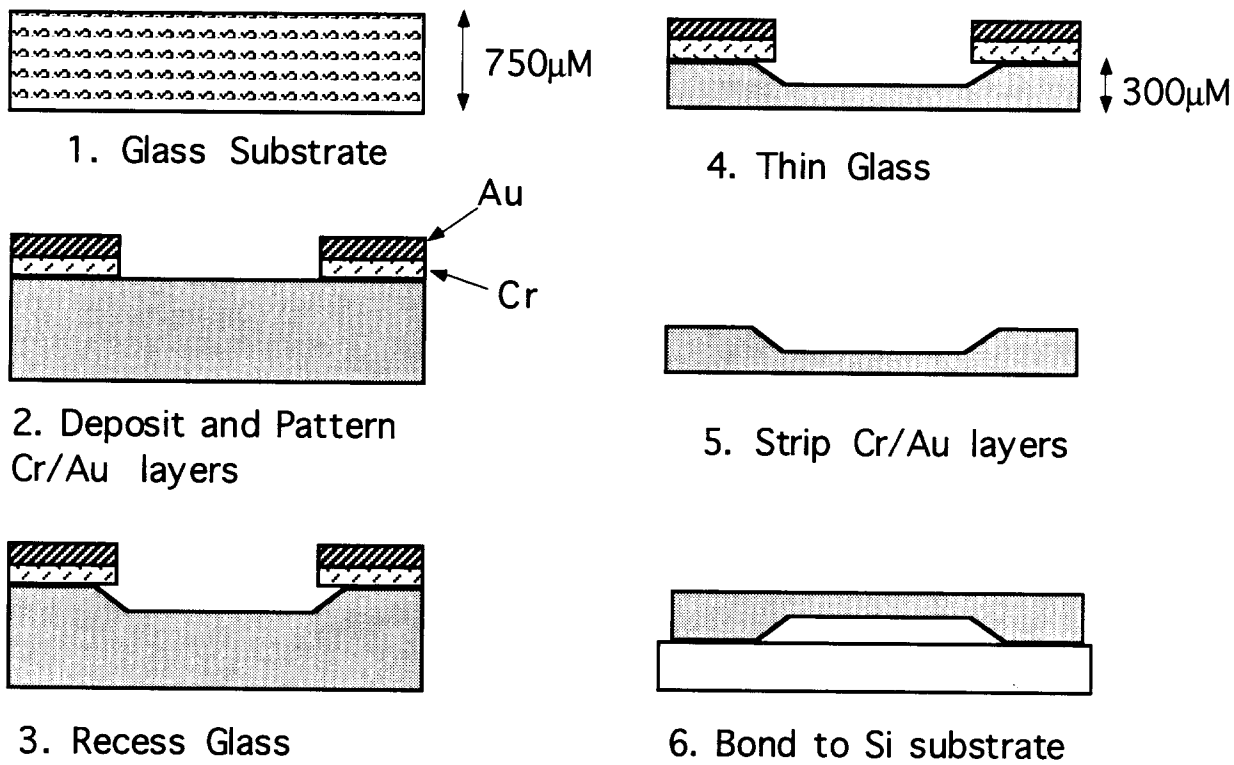

Figure 6: The fabrication sequence for making a low profile package.

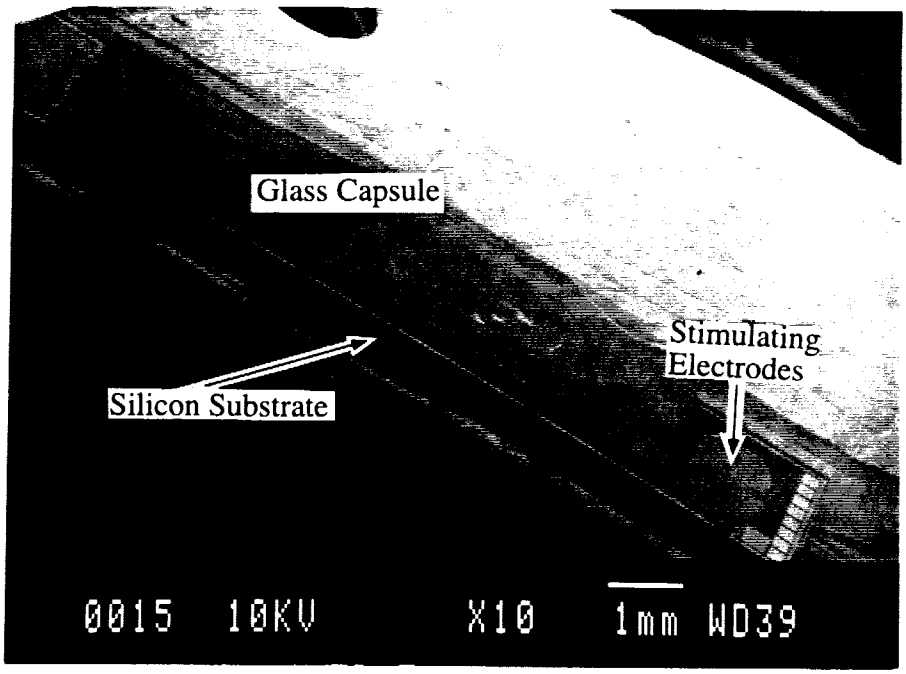

Figure 7: The SEM micrograph of a low profile glass package.

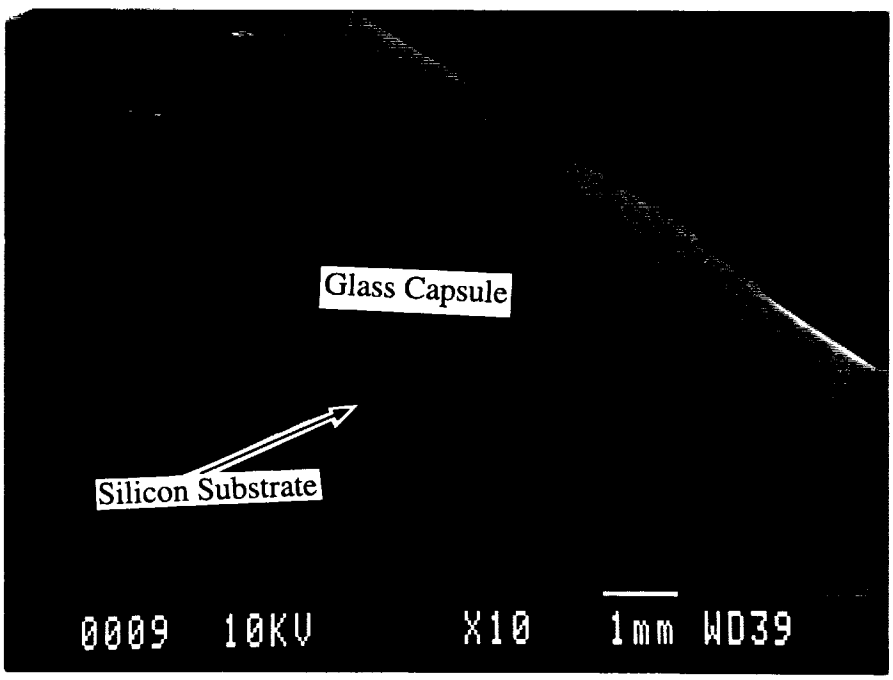

Figure 8: The SEM micrograph of the regular microstimulator package.

2.1.5 In-Vivo Tests

The devices that we have prepared and sent to Vanderbilt University during the past quarters are still being implanted in several animals. More data from these tests will be reported in future progress reports when the devices are harvested for biocompatibility testing. This quarter, we have fabricated a prototype low profile package by recessing glass and have prepared 4 samples. To learn more about the mechanical integrity and also the biocompatibility of these samples, we have sent these 4 devices to Dr. Mark Humayun at Johns Hopkins University. They have already started to implant these devices into animals. From this set of new implants we hope to obtain information about our package in the coming months and report them in our future progress reports.

2.2 Status Of Microstimulator Circuitry

At the end of the previous quarter, we had very recently finished a new CMOS fabrication run for new microstimulators. As detailed in a previous quarter report (two quarters ago), the objectives of this new run were to improve the circuitry's performance in certain ways and to provide more microstimulators for assembly. Specifically, the intended improvements to the circuitry were principally the following: (1) lower power consumption, about 50% less than the previous generation, for improved reliability in telemetric powering; (2) more stable stimulus current, since undesirable variability had been encountered in the previous generation's stimulus current; and (3) a greater range of stimulus currents, from less than 1mA to about 50mA from a single device, instead of a fixed, nominal 10mA in the previous design. The reduction in power consumption would result primarily from a reduction in current used in the voltage regulators (4.5V and 9V supplies), obtained by using redesigned, smaller junction area Zener diodes. The principal blocks of the circuitry otherwise remained essentially the same, with at most minor changes in design and no important change in functionality. These blocks were tested and found to work as expected.

However, it was quickly observed that all of the circuits resulting from this latest fabrication run (including single and multichannel microstimulators) seemed to be suffering from unexpectedly high leakage currents. The problem was found to be especially serious on the microstimulator, since the input voltages tend to be relatively high in order to get stably working 9V and 5V supplies. For instance, in the microstimulator, the total leakage current can easily reach several tens of mA for an input voltage (single-ended) of 10V, instead of the 1.5mA expected current. Immediately we began the process of determining the source of this leakage.

We have performed a large series of other tests on these chips, and although we have identified some *potential* causes of this high leakage, we still cannot pinpoint the main source of this problem. This has been a very frustrating process for us, especially since we still have not been able to find the culprit. However, we will continue to test the circuitry until we can determine where this large leakage comes from. Although we have not yet found the source of leakage, a number of tests were performed that could rule in/out some possible causes, as discussed below.

Thus far no specific circuit design flaw has been identified in the microstimulator. In addition, it was found that reverse junction leakage was not large enough to account for the high leakage current in the microstimulators. However, we were initially concerned that parasitic structures could be playing a role in the leakage observed. For instance, it was necessary to be sure that significant reverse junction leakage was not occurring between the N-epitaxial regions and the surrounding deep-boron-diffusion isolation structures. It was also necessary to be sure that parasitic PNP bipolar transistors were not turning on and causing latchup or a related state. These PNP structures result naturally from P+ active regions or P-wells in N-epi, with the P-substrate and deep-boron-diffusion regions acting as a common collector. Additionally it was a concern that

if the N-epi had too low of a concentration, punchthrough could occur between the p-well and the p-substrate. Surface leakage was also a possibility if for any reason there was ionic contamination between active regions.

To investigate these possibilities, we sent samples of the chips to be analyzed with the spreading resistance technique. This technique gives us an accurate doping profile of the chips' cross-section, limited to a small zone of interest. From this information we determined depths and doping levels of the source/drain implants and P-wells, the thickness and doping of the N-epitaxial layer, and the doping level of the P-substrate. We also did an analysis of chips from the previous CMOS run for comparison and found that the profiles were not significantly different, though not identical. Using this data the parasitic bipolar devices' (P-well/epi/substrate) forward current gain was found to coincide with experimentally measured results: about 4 to 12 depending on the base current levels. This is a bit better than one might ideally desire, but the possibility of punching through the parasitic "base" (N-epi) was essentially eliminated at the voltage levels typically encountered on the microstimulator, and furthermore the parasitic bipolar devices should never turn on under normal circumstances. Measurements of the MOS devices and field inversion transistors indicated that surface leakage is not a problem.

The circuit chips were sent out for a thermal scan, in which an input is applied and the flowing currents cause certain areas to heat up and to be easily visible with an infrared camera. It should be noted, however, that the resulting "hot spots" do not necessarily indicate the precise leakage zones but rather low resistance paths that are connected to these leaky areas and hence are robbing some of the leakage current. In the case of the microstimulator, there were no consistent hot spots. This supports the data that indicate that there is not a specific circuit design flaw.

Another possible source of leakage could be current leakage through the field oxide. It was observed that high currents often seemed to flow in two particular areas of the chip. The common factor that these zones seemed to have is that they are areas where polysilicon passes over deep-boron-diffusion isolation (DBD) and is insulated from the DBD by field oxide. One of these areas was isolated for further study and is shown in Figure 9. It can be seen that there appears to be a twisting dark line within the polysilicon (center of the photograph). Indeed this was one of the characteristics that made this likely area easier to spot, because it was typically observed that an irregular flaw of this sort would begin to get accentuated as the input voltage and current consumption rose. The potential at this polysilicon zone is only a diode drop below the input voltage, after a rectifying diode. Typically at an input of 3-5V it was possible to observe about 10mA of current consumption, and by isolating this area with laser cuts it was possible to see that typically at about 10V applied to the poly with the DBD grounded as in actual operation, breakdown was irreversible and much larger currents would flow. The result after breakdown was measured to be a very low resistance path, typically less than 100Ω. Furthermore, it can be seen in Figure 10 that this twisted flaw is not visible in a SEM photograph. This implies that it is a subsurface feature, as would be expected if the problem is indeed in the poly to field oxide interface. When the voltage was swept between poly and DBD in this case, the resulting trace had the characteristics of a diode with a very leaky reverse behavior, a sharply defined forward turn-on voltage, and a reverse breakdown of about 7-10V. In the microstimulator, this "junction" would be in effect operated in the reverse-biased region. The data would seem to indicate that the polysilicon may be touching or almost touching the DBD, through a defect in the oxide.

One possibility that was postulated was that the field oxide was very thin and breaking down easily. However, after direct measurement of the field oxide thickness, it was found to be 0.6-0.8μm thick, as expected. Unless there are substantial defects ad pinholes in the oxide, one should not expect any leakage current in the film; we do not see any major problems in terms of defect density and pinholes in our field oxides, although this needs to be further studied. In studying the same suspect poly bridge on other dice, it was observed that the poly did not *always* break down or seem leaky over deep-boron-diffusion regions.

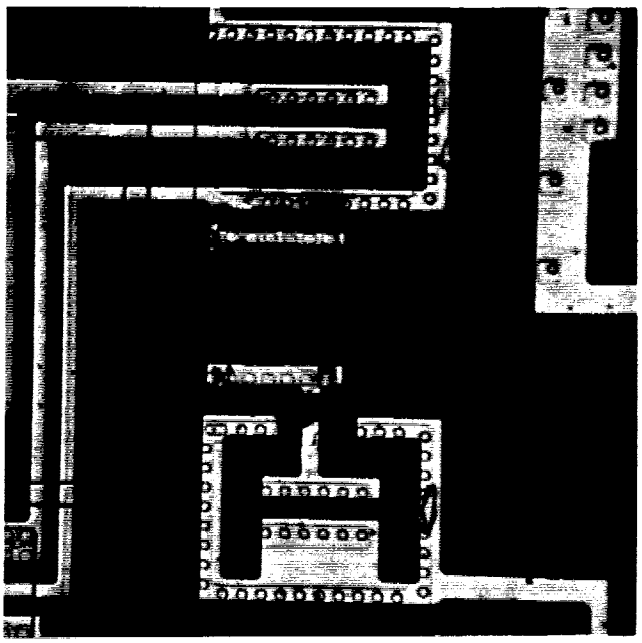

Figure 9: An area where field oxide seems to have broken down between polysilicon and deep-boron-diffusion isolation. Note the twisted, dark flaw in the center of this optical photograph.

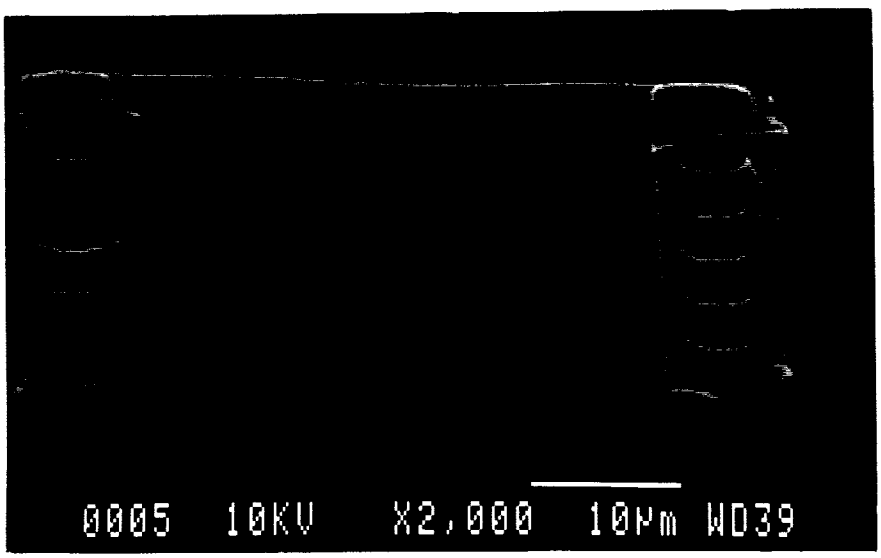

Figure 10: Close-up of the isolated poly bridge over DBD.

In spite of all of the testing that we have performed (the details of much of this testing has not been presented in this report because of space limitations) on a large number of dice, we still cannot explain why the majority of the microstimulator chips have a substantial leakage current. It should be noted that many of the test devices, and even some of the test circuits, operate correctly and do not show this leakage current. However, the microstimulator circuitry does generally show a high level of leakage. As mentioned before, we will continue our testing and we will find the source of this leakage so that we can proceed and fabricate complete microstimulators. We will present the result of this testing in the next report.

2.3 Packaging and Microtelemetry For Next Generation Microstimulators

The single-channel microstimulator that has been under development for the past few years by our group, as well as others, is about three orders of magnitude smaller than conventional implantable stimulation units that use hybrid thin-film technology. As part of our contract goals, we are required to develop miniature packages for a variety of implantable neural prostheses. In order to minimize the size of these packages, we have been examining ways to reduce the volume of implantable stimulators by another order of magnitude. Figure 11 illustrates how this drastic size reduction can be achieved. By far the largest components in the microstimulator system are the charge storage capacitor and the discrete receiver coil. These two components take up about 90% of the total microstimulator volume. As shown in Fig. 11, the volume of the microstimulator can be reduced by an order of magnitude by integrating the receiver coil directly on the CMOS substrate and by not using a charge storage capacitor. While the microstimulator is currently about 2.5 mm thick and has a volume of about 50 mm^3, a system with an integrated coil and no charge storage capacitor will be in the 300 μm to 500 μm thickness range and have a volume of about 6 mm^3. We call these extremely low volume FES systems mini-microstimulators.

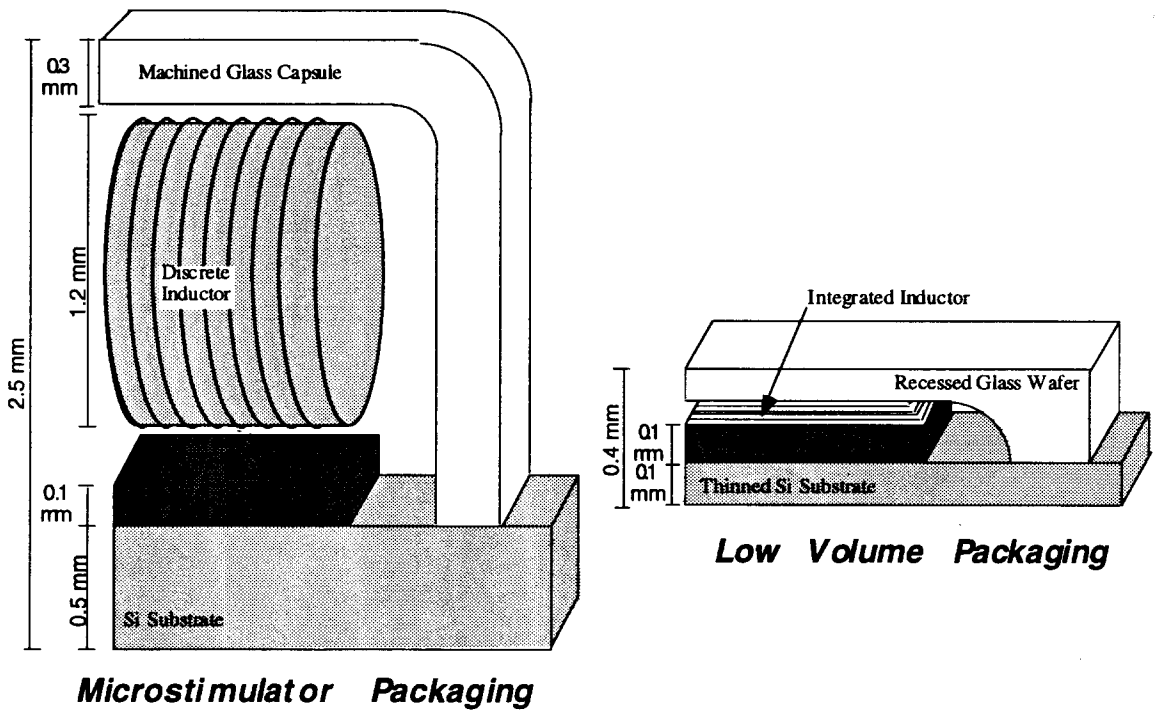

Figure 11: A scale drawing comparing the microstimulator with a mini-microstimulator.

We are developing a nerve cuff stimulation system to demonstrate the feasibility of a telemetry powered mini-microstimulator. Stimulating nerve cuffs are a particularly well suited application for a mini-microstimulation device because they need relatively low current levels. Typical stimulation levels for nerve cuffs are 100 μA to 2 mA, which is a good fit with the 3 mA output that our experiments have shown is feasible using on-chip coils and no charge storage capacitor (for comparison the microstimulator stimulates with an output of 10 mA or more). Figure 12 shows a photograph of some of the on-chip receiver coils that we have fabricated and tested, Table 5 summarizes the specifications for the 8-channel nerve cuff system which we are developing, and Figure 13 is an exploded view of what such a system will look like. Note that the nerve cuff and electrodes can be either integrated directly with the circuitry hermetic packaging substrate, or the nerve cuff could be attached by a connector.

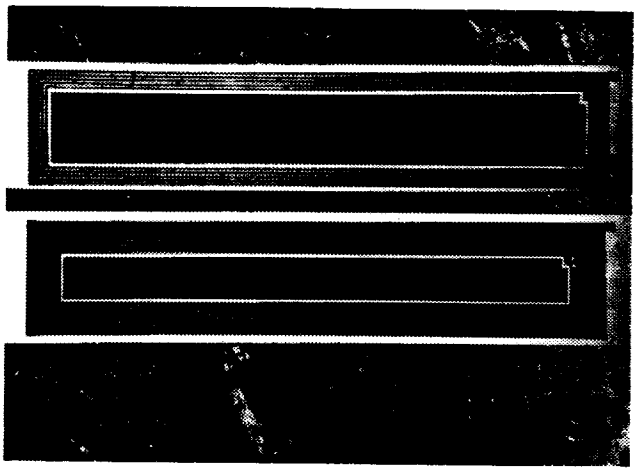

Figure 12: Photograph of 5 and 10 turn Cu on-chip coils with NiFe cores. These coils are 2 by 10 mm.

Table 5: The specifications for a telemetry powered stimulating nerve cuff.

8-Channel Peripheral Nerve Stimulation System Specifications

General

Dimensions = 2.0 mm X 10 mm X 0.5 mm	Power Delivery = Telemetry
Power Consumption < 15 mW	On Chip Regulated Supply = 4 Volts, Gnd

Telemetry Link

Receiver Coil = On-chip (2.2mm X 10mm)	Range = 3 cm
Transmitter Coil = Planar, air core (80 mm dia.)	Carrier Frequency = 4 MHz
Modulation Frequency = 1 kHz to 50 kHz	

Stimulation

Output Channels = 8	Amplitude = 0 to 2 mA (100 μA steps)
Duration = 0 to 2047 μS (1 μS steps)	Stimulation Protocol = Bi-phasic
Frequency ≤ 50 Hz	Output Load < 1.5 KΩ

During the past quarter significant advances have been made in the areas of on-chip coils and low power receiver circuitry for use with the on-chip coils. Improved on-chip coils have been designed, fabricated and tested this quarter, and they showed a substantial improvement in the amount of power that they can pick up. The best new coil design has over twice the inductance of earlier coil designs. These new receiver coils should reduce the RF field needed to power mini-microstimulators and they will half the required tuning capacitance (The 1nF tuning capacitance required for the original on-chip coil design took up almost 4 mm^2 of die area). This quarter we also performed extensive testing on the RF receiver circuitry for use with these on-chip coils. We have found this circuitry to be functional, although its current consumption was about an order of magnitude higher than it was designed to be. The cause of this excess current was identified this quarter, and it is easily corrected.

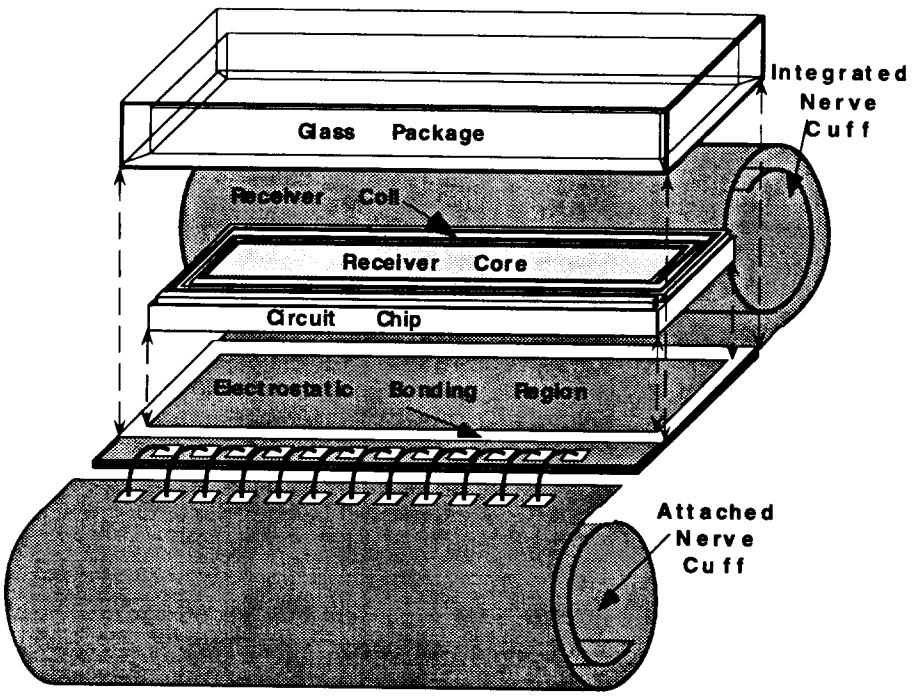

Figure 13: One mini-microstimulator application is this nerve cuff. The nerve cuff can be either integrated directly with the packaging substrate, or attached by a connector.

2.3.1 Test Results On CMOS Circuitry

In our last quarterly report we mentioned that we completed fabrication of the first iteration of RF receiver circuitry designed to operate with on-chip coils. As we reported, we performed preliminary tests on this circuitry and found that it was functional, however it consumed about an order of magnitude more current than expected. During this quarter we performed extensive testing on this circuitry, and have identified the cause of the large current consumption, which is easily correctable. Figure 14 shows a die photograph of the RF receiver circuitry, which was designed specifically to operate with our on-chip coils. This circuit includes a 4 MHz tuned RF receiver, a 4 V supply generator, a 1 MHz system clock recovery circuit, and a 50 kHz data demodulator. There are several differences between this circuitry and the single channel microstimulator circuitry, most importantly these circuit blocks have been re-designed to consume about half of the power of the first generation microstimulator circuitry.

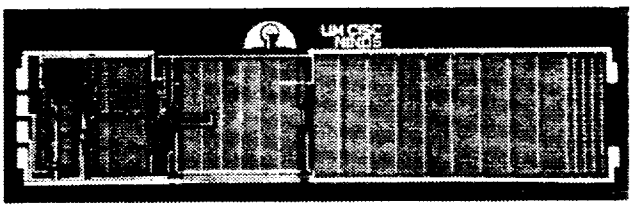

Figure 14: Photograph of the integrated RF receiver circuitry for use with on-chip coils. This 1.29x5.78 mm circuit includes a 4 volt generator, a data demodulator, and a clock recovery circuit.

In spite of its large current consumption we were able to operate this circuitry telemetrically using an on-chip receiver coil. For testing, we connected a planar 15 turn transmitter coil to a battery powered class E transmitter tuned to 4 MHz. A 10 turn electroplated receiver coil was connected by wirebonds to the RF receiver circuitry chip, and the receiver coil was placed 0.5 cm away from the transmitter coil. Figure 15 shows output of the 4 volt generator. As can be seen, this supply has abut 350 mV of ripple, which is mostly due to the unexpectedly high current draw of the system. Figure 16 shows the 1 MHz clock generated from the 4 MHz carrier. The ripple on this clock is due to the ripple on the 4 volt generator which powers the clock. Figure 17 shows the recovered data envelope. The recovered data envelope also has ripple due to the ripple of the 4 volt generator that powers it, but the 4 MHz ripple is too fast too see on the 10 kHz data envelope shown in Fig. 17. Because these tests were performed with a relatively inefficient 10 turn copper electroplated receiver coil without a core, and because the RF receiver circuitry was consuming an order of magnitude more power than it was designed to, the link distance had to be kept down to a distance of 0.5 cm, and the load current had to be kept below 1mA.

Although the RF receiver circuitry for use with on-chip receiver coils was functional, it consumed about an order of magnitude more current than it was designed to. This large current drain limited the telemetry range at which this circuitry could be powered in our tests, and added ripple to the output of the on-chip 4 V supply generator. In order to localize where this current consumption was occurring, thermal images of the circuit were taken during operation. Thermal imaging is a standard technique for mapping power consumption in integrated circuits. The principle of this technique is that the more power an area in a circuit is taking, the more that area heats up. The thermal images of the RF receiver circuitry clearly show one localized hot area in the data demodulation circuit. Figure 18 is one of the thermal images of the RF receiver circuitry showing this hot area where most of the power in the system is being consumed. After the thermal images were taken, the layout of the data demodulator was examined closely to find why so much power was being dissipated there. A layout error was quickly found that accounted for the excess current draw.

Figure 19 shows the layout error in the on-chip coil RF receiver circuitry. The circled transistor is a current source which together with capacitor C1 forms a low pass filter. The circled p-FET transistor was incorrectly laid out such that the body of this transistor was connected to the 4 V supply rather than the transistor's source. This is an easy mistake to make since the body of most p-FET transistors are routinely connected to the 4 V supply. However the circled transistor is at the input to the data demodulator, and since this input is the rectified received RF signal, it is always a higher potential than the 4 V supply. The result is the source to body diode turning on and consuming sizable current. The body of this FET was supposed to have been connected to the source rather than the 4V supply. This would have ensured that the source to body diode never turned on. This layout error can be easily corrected by a simple change in the metal mask.

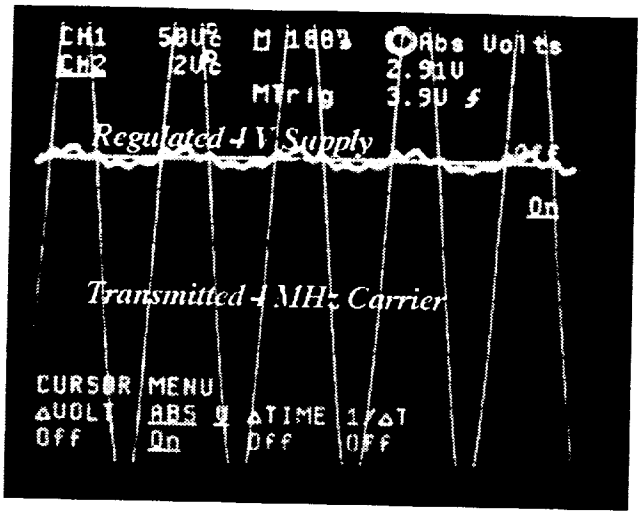

Figure 15: The regulated 4 Volt supply generated by the integrated receiver circuitry with an electroplated receiver coil.

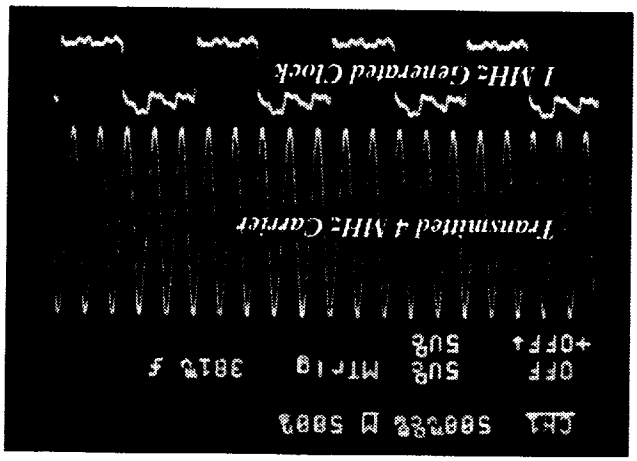

Figure 16: The 1 MHz system clock generated from the received RF signal by the integrated receiver circuitry with an electroplated receiver coil.

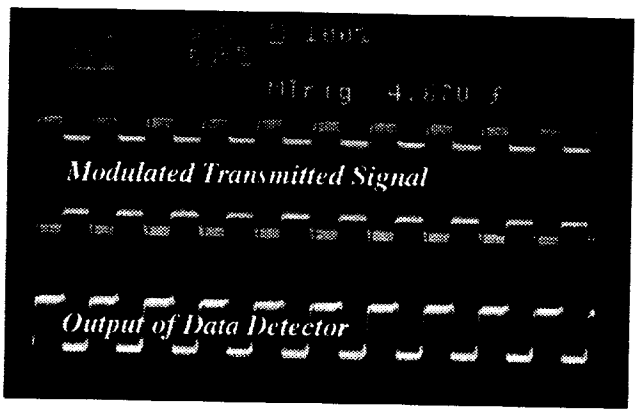

Figure 17: The data envelope recovered from the received RF signal by the integrated receiver circuitry with an electroplated receiver coil.

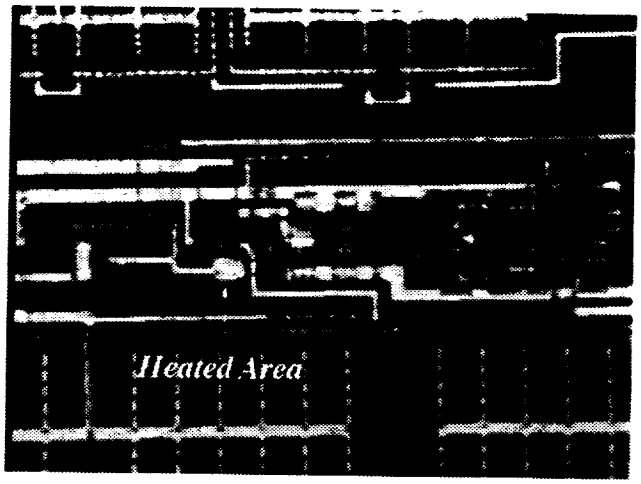

Figure 18: A detail of a thermal image of the circuitry during DC operation. The heated area marked in the picture is consuming the majority of the chip's power.

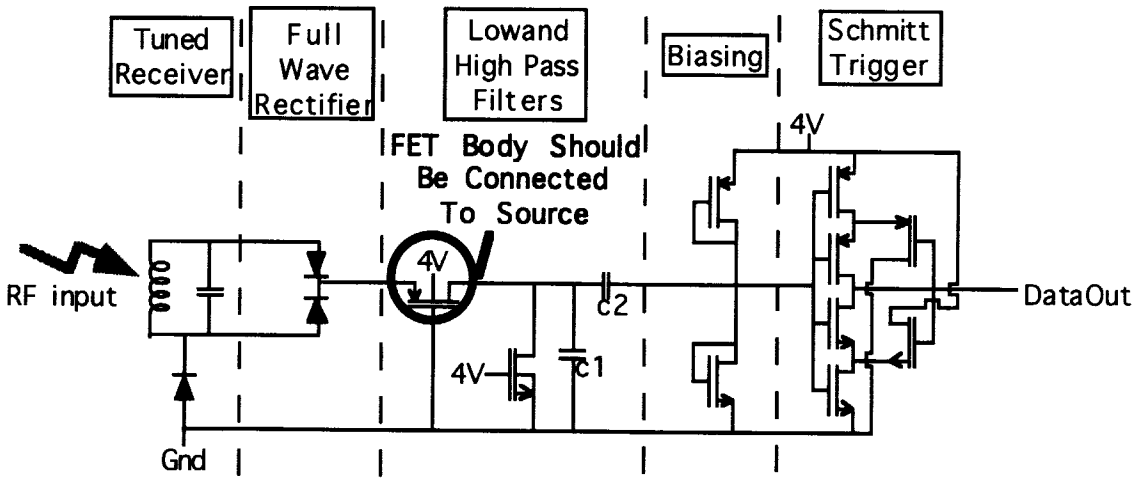

Figure 19: The envelope detector as it was incorrectly laid out in the on-chip coil receiver circuitry. The body of the circled p-FET should have been connected to its source rather than the 4V supply. The source of this FET is connected to the received RF signal which always peaks at a potential above the 4V supply.

Although we have not yet corrected the layout error in the on-chip coil receiver circuitry, we have cut out the improper connection with a laser. Cutting out this error results in a circuit that consumes about the same amount of current as if the error was corrected, however it leaves the envelope detector non-functional. Figure 20 compares the current consumption of the on-chip coil receiver circuitry before the layout error was cut out, and after it was cut out. As can be seen in this figure, the current consumption of this circuitry drops by a factor of about 5 when the layout error is cut out. However, our testing has revealed that the layout error in the data detector it is not the only cause of excess current draw. Even when the layout error is cut out, current consumption for the circuit is still about a factor of 2 higher than designed. The behavior of this circuit after the layout error is cut out is very similar to the behavior of the microstimulator circuitry as discussed in section 2.2. This is not surprising since both the microstimulator circuitry and the on-chip coil

receiver circuitry were fabricated during the same fabrication run on the same silicon wafers. In both of these circuits the problem has been traced to a leaky oxide with a low breakdown voltage between the 1st layer polysilicon and the deep boron diffusion, as mentioned in section 2.2.

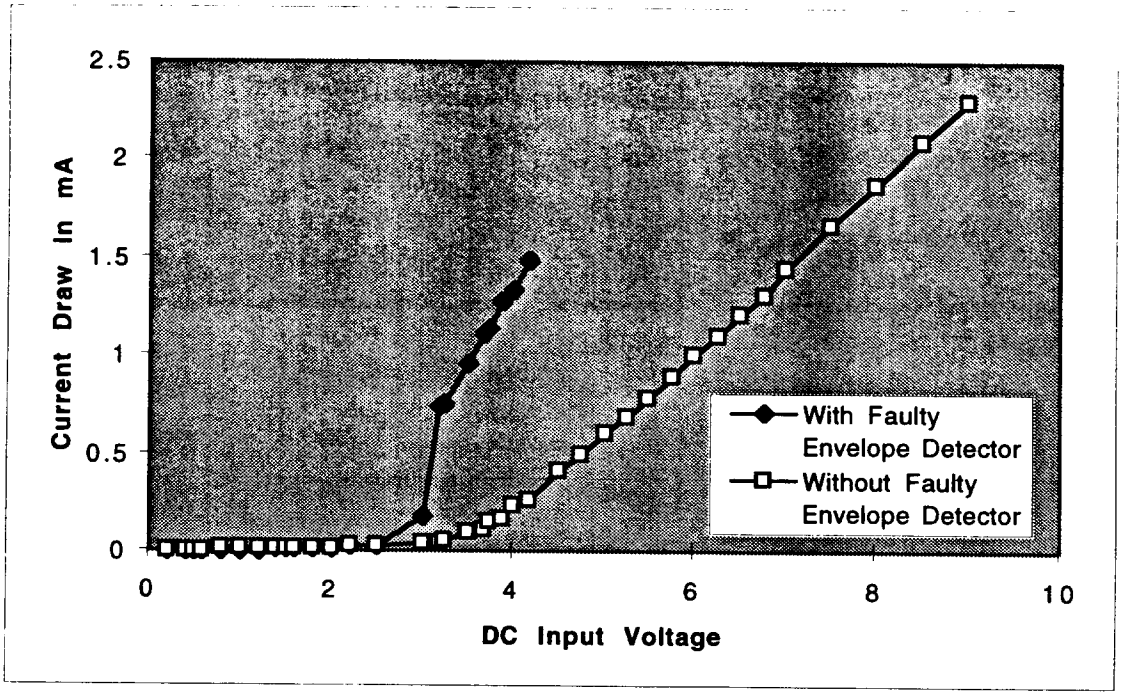

Figure 20: The current consumption of the cuff circuitry as a function of the input voltage. Current measurements are shown both before the layout error is cut out, and after the layout error is cut out.

It is important to point out that the successful telemetry tests with the on-chip coils shown in Figures 15, 16, and 17 were carried out with receiver circuit die on which both the layout error and the leaky dielectric problems had not been corrected. This means that the current consumption of the die in these figures were approximately 4 mA when they should have been less than 0.5 mA. In spite of this large current consumption, it was still possible to power these circuits through a 0.5 cm telemetry link using on-chip receiver coils which were low efficiency designs without cores. We are confident that circuitry with the correct current consumption combined with our higher efficiency coil will allow us to power implant over much larger distances.

2.3.2 Improved Coil Design

This quarter we designed and fabricated new on-chip coils which are capable of receiving more power than our original on-chip coil design (we reported on the original coils in the last quarter report). The new on-chip coils have two improvements over the original design. First, the original design had a large space in the middle of the windings for an electroplated core as illustrated in the left half of Figure 21. However, our experiments show that the coils which performed best are that planar coils with cores underneath copper windings, as illustrated in the right half of Figure 21. Since these coils do not need space for a core in the middle of the windings, there is room to increase the number of turns without increasing the coil dimensions. A second way that the new coils were made more efficient is by using a slightly more aggressive pitch on the coil windings. This also allows for a few more turns without increasing the coil

dimensions. It should be mentioned that tighter pitch windings and increased number of turns will not only result in coils with higher inductances, but also with higher parasitic resistance (which degrades the coil's Q). Simulations and measurements show that for these new coil designs the efficiency of the telemetry link has increased with the inductance in spite of this degradation of Q. Table 6 lists the new coil designs and their expected inductance and Q for the case of an air core. With a NiFe core underneath the windings, the both the values for the inductances and the values for Q should be about a factor of 3 higher.

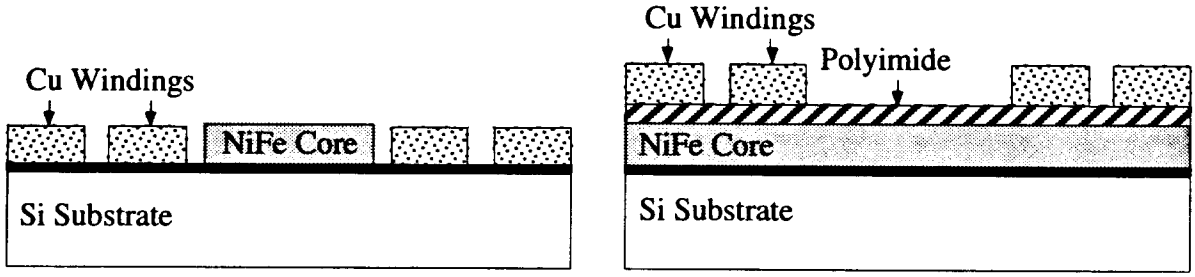

Figure 21: Two structures for planar on-chip receiver coils with cores. Our experiments have shown that the design on the right is a more efficient receiver coil.

Table 6: The new coils which were designed, fabricated and tested this quarter.

Number of Turns	Core Material	Dimensions	Pitch	Expected Inductance	Expected Q of coil
13	air	2.0 by 10 mm	70 μm	1.26 μH	2.94
15	air	2.25 by 10 mm	70 μm	1.63 μH	3.33
17	air	2.0 by 10 mm	55 μm	2.01 μH	2.90
19	air	2.25 by 10 mm	55 μm	2.55 μH	3.29

The new coil designs described in Table 6 were fabricated and tested this quarter. Both samples with NiFe cores and samples with air cores were fabricated (the air core samples are for evaluating geometrical improvements in coil design without added variables such as core thickness and core quality). Table 7 shows measurements from these new coils. The inductance of the air core version of these coils depends on the number of turns, but the best of these coils has over twice the inductance of our original coil design. However, the inductance of these coils are about 20% lower than the predicted value given in Table 6. This is because the coils measured for Table 7 have a electroplating thickness of only about 3 μm rather than our target of 10 μm electroplating thickness. When thicker coils are made in the next few weeks they should have inductances and quality factors very close to those in Table 6.

Table 7: The new coils which were designed, fabricated and tested this quarter.

Number of Turns	Core Material	Dimensions	Measured Inductance
13	air	2.0 by 10 mm	1.04 μH
15	air	2.25 by 10 mm	1.32 μH
17	air	2.0 by 10 mm	1.58 μH
19	air	2.25 by 10 mm	1.95 μH
13	NiFe	2.0 by 10 mm	1.49 μH
15	NiFe	2.25 by 10 mm	1.90 μH
17	NiFe	2.0 by 10 mm	2.34 μH
19	NiFe	2.25 by 10 mm	3.07 μH

This quarter we also experimented with fabricating electroplated receiver coils on a wafer made out of commercial ferrite material rather than silicon. Coils fabricated directly on a ferrite substrate will be as small as coils on a silicon substrate, and yet these coils will have higher inductances and quality factors. This is partly because commercial ferrite material has higher permeability and less eddy losses than the electroplated NiFe which we currently use as a core on on-chip coils, and partly because the ferrite substrate is geometrically much thicker (about 200 μm) than the 10 μm electroplated NiFe. Receiver coils on a ferrite substrate might be ideal for mini-microstimulator applications which require the stimulator to be implanted deep in the body and hence far from the transmitter (more than 3 or 4 cm), or mini-microstimulator applications requiring large stimulating currents (more than about 3 mA). However, coils on a ferrite substrate cannot be integrated on the same substrate as receiver circuitry such as the on-chip electroplated coils can. This means that a system with a receiver coil on a ferrite substrate would have to be hybrid attached to circuitry, making these systems larger and more complicated to assemble than fully integrated systems. This quarter we ordered wafers machined out of a commercial nickel zinc ferrite material with a relative permeability of 125 at 4 MHz. These wafers proved to be very brittle, and difficult to work with, but we hope to be able to fabricate and test coils fabricated on these wafers in the coming quarter.

3. ACTIVITIES PLANNED FOR THE COMING QUARTER

Our efforts on the various aspects of this project will continue in the coming quarter. First, we will continue our soak tests of glass-silicon packages and we hope to be able to start some new tests in this quarter. These tests will be performed on both the large and the flat glass package. We are still developing techniques by which we can overcome or circumvent the problem of silicon dissolution in saline solutions at high temperatures. Once this is done we will be able to conduct additional tests at high temperatures. In-vivo tests using the silicon-glass packages will also continue and we will report on the results of these tests as they become available.

In the area of microstimulator development and testing, our main objective remains to be the determination of the source of high leakage current in our latest batch of devices. A large number of tests have already been performed, and another series of tests will be carried out to determine the source of this problem. We hope to be able to correct the problem and start another fabrication run if necessary.

Finally, in the coming quarter we will design and layout the entire nerve cuff mini-microstimulator circuitry. Up until now we have designed, fabricated and tested only the critical analog front end of this system's circuitry (which includes the on-chip receiver coil, the RF receiver, the power generator, the clock, and the data demodulator). The remaining circuitry that still needs to be designed is the digital circuit block and the stimulating output circuit block. The digital circuit block includes an 11-bit counter, a 41-bit data register, a 32-state finite state machine, and various control logic, and the current output block includes the programmable output current generator as well as the output de-multiplexers. We plan to fabricate this complete mini-microstimulator system this spring. Also during the coming months we will continue improving the efficiency of the on-chip receiver coils.